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A Capacitance-Size Diagram for Embeddable Capacitance

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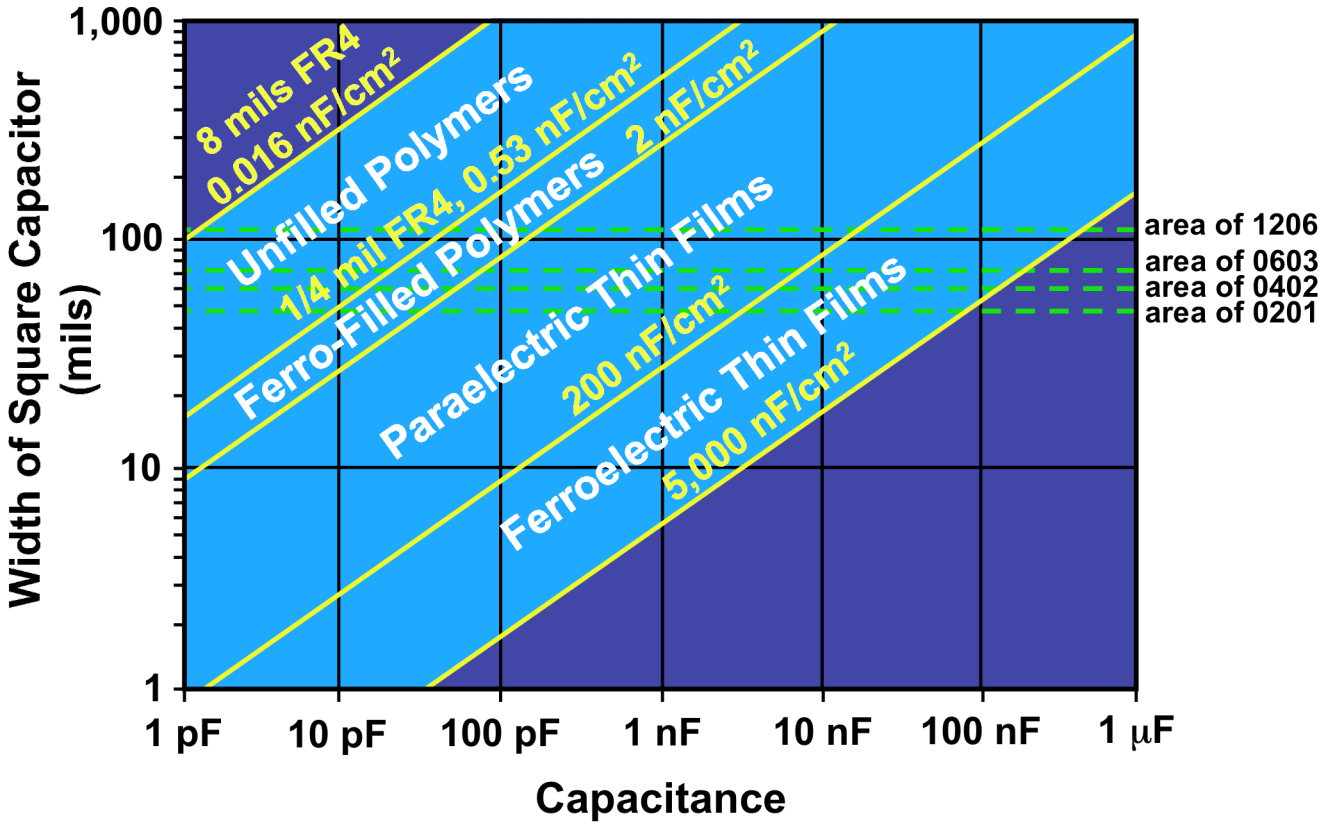
In the past few columns, I've been describing some of the commercially-available embeddable dielectric technologies and why they act they way they do. In this installment, I want to pull together the capacitance data into one place. One of the most basic questions in designing a part with embedded capacitance is "How big does the cap have to be to give XXX nF?" Of course, you can get there by calculating the specific capacitance for a given embeddable dielectric technology from:

$$\text{Specific Capacitance, nF/cm}^2 = 0.885 \frac{\text{Dielectric Constant}}{\text{Dielectric Thickness, Microns}}$$

But we're visually-oriented creatures, so it's easier for us to grasp relationships if we can see them all in one place. To give a quick approximate answer to this question, I plotted this equation in useful units for the major embeddable technologies to make the diagram below.



It's fairly self-explanatory. You find the capacitance you want on the X-axis, go straight up till you get to the dielectric you want, then turn left and read off the Y-axis. Assuming that the cap is square, this will be the length of one side in mils. Or, if you want the capacitance per square

inch for board-level calculations, just move along the top of the graph to the dielectric you want, and go straight down.

There are four bands corresponding to the four major technologies currently available. Starting at the top, we have the unfilled polymers. In principle, these have no upper limit of thickness, but I chose to start off with 8 mils and end up with 1/4 mil, which gives a maximum for this technology of about half a nF/cm^2. Next we have polymeric films containing finely-divided ferroelectric powders, which are capable of up to 2 nF/cm^2. These two technologies are in use today as distributed decoupling capacitance between the power and ground layers over the entire board. I searched the websites of advertised products in these two categories, and they all fit in their respective bands.

Paraelectric thin films would include sub-micron layers of materials such as SiO_2, Al_2O_3, Ta_2O_5 etc. These can be formed by methods more familiar to IC manufacture such as CVD, sputtering and sol-gel, but plenty of high-value discrete caps have been made by anodization, and that can work for embedded caps too. Anodizing Ta at 125 V will give 2000 A of oxide with a specific capacitance of about 100 nF/cm^2. The most you could get out of this approach, avoiding excessive defects and providing reasonable breakdown voltage, is probably around twice that. IC gate electrode research is a rich source of information for these thin film materials. Ferroelectric films, by virtue of very high k, have been demonstrated on FR4 with 5000 nF/cm^2 and might even be able to improve a little on that. If you don't see your favorite dielectric on there, you can interpolate. This is all fairly approximate and log-log coordinates allow small uncertainties to be relatively unimportant.

Clearly, no one dielectric can be used over all six orders of magnitude of value range; this would require three orders of range in size. It might make sense to use the thick FR4, which is present in the board anyway, as the dielectric in small-valued caps and a more exotic technology for the large-valued units. The low-value caps used in applications such as A/D converters, filters and timing tend to require tighter tolerance and less leakage than larger-valued caps used for decoupling and energy storage. For once, mother nature plays into our hand since the lower-k dielectrics tend to be more stable against frequency and temperature, and exhibit generally less leakage than the high-k ferroelectric materials.

For the sake of comparison, I've included the areas of four popular sizes of discrete components, along with a 10 mil keep-away distance around them, expressed as if they were also squares. But it is not necessary for every embedded cap to be smaller than its surface mount counterpart. The goal is to free up surface area and a larger cap, within reason, can go underground to accomplish this.

Capacitance isn't everything, of course. For decoupling, the issue is more about inductance and the ability to deliver charge rapidly to where you need it, but we'll leave that for a future column. Hopefully, this diagram will help give a quick general idea of the dimensions required for your applications.